

Figure 7.1: PriorArt

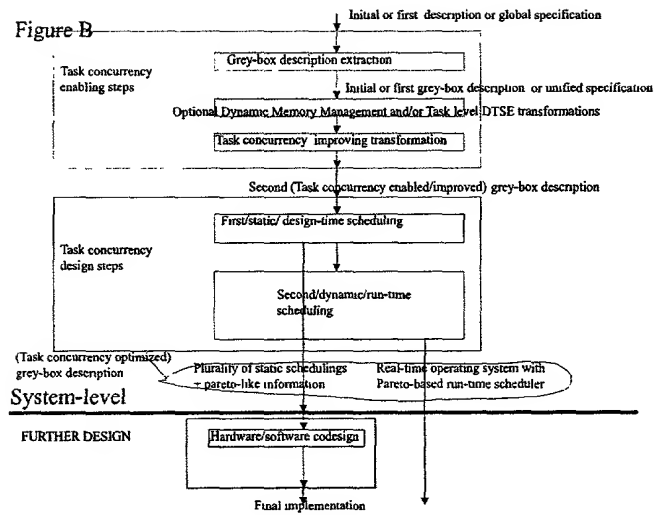


Figure 7.2: TCM overview

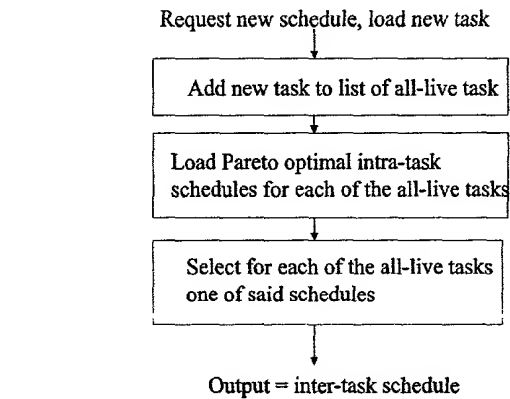


Figure 7.3: TCM run-time scheduler

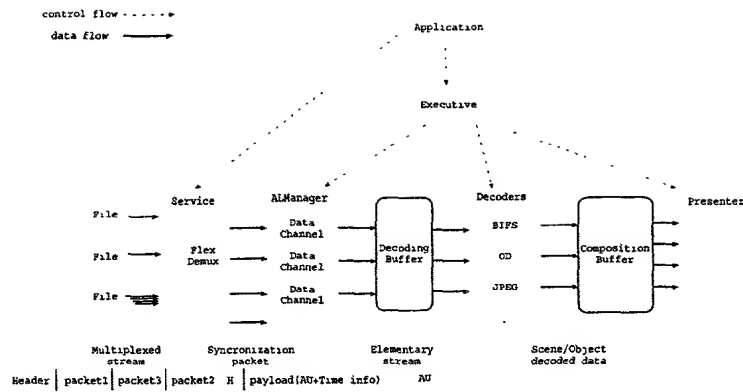


Figure 7.4: System layer of MPEG4 IM1 player, with several concurrent modules and complex dynamic control constructs.

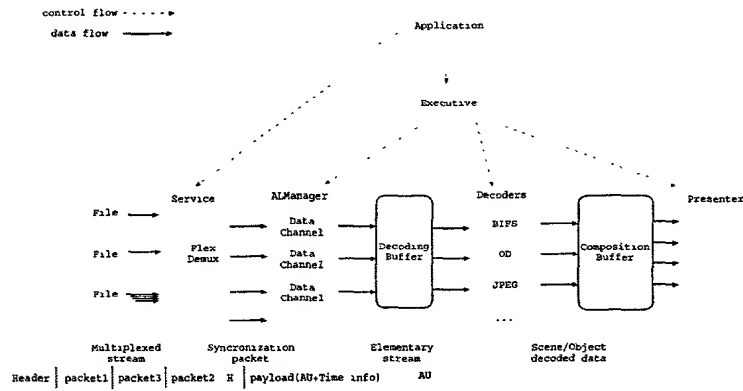


Figure 7.5: System layer of MPEG4 IM1 player, with several concurrent modules and complex dynamic control constructs.

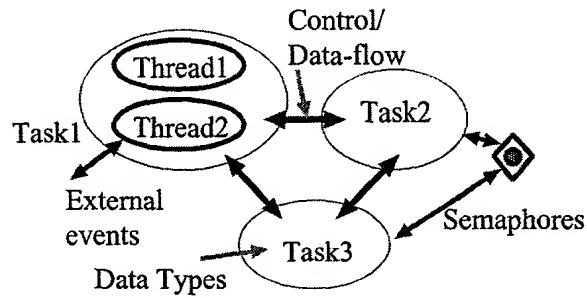


Figure 7.6: Illustration of important grey-box model elements.

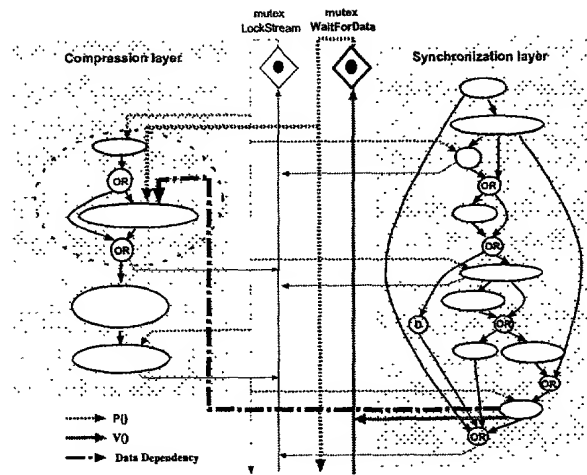


Figure 7.7: A real-life example of a grey-box model extracted from system layer of the MPEG4 IM1-player.

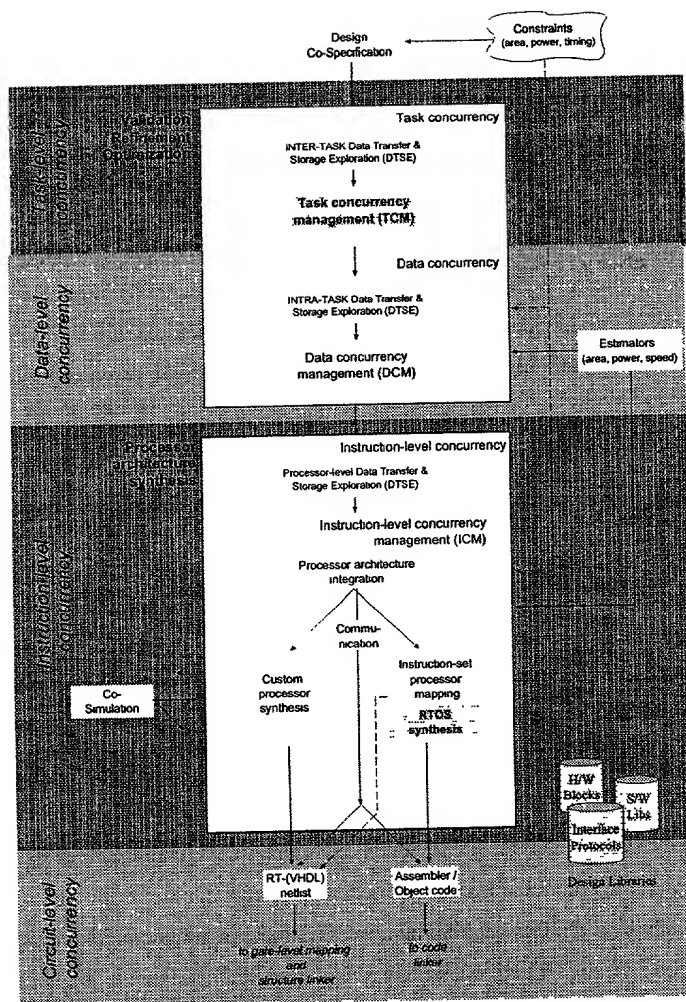


Figure 7.8: A global unified system design methodology covering different levels of abstraction with emphasis on the concurrent task related context.

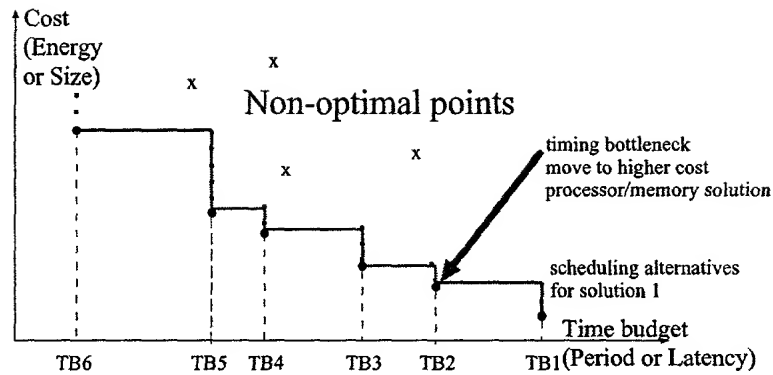


Figure 7.9: Global Pareto curve after TCM scheduling and processor allocation/assignment exploration

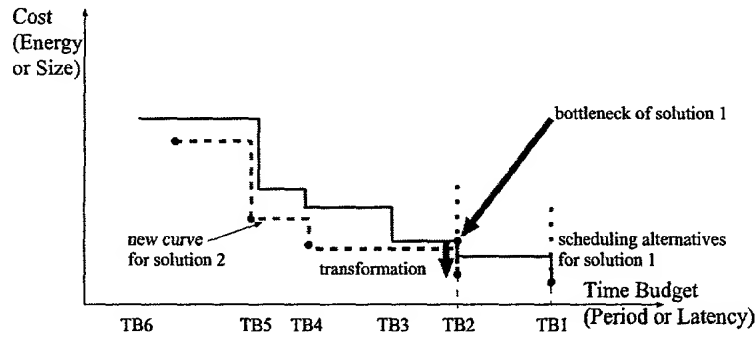


Figure 7.10: Global Pareto curve after TCM concurrency extraction and transformations

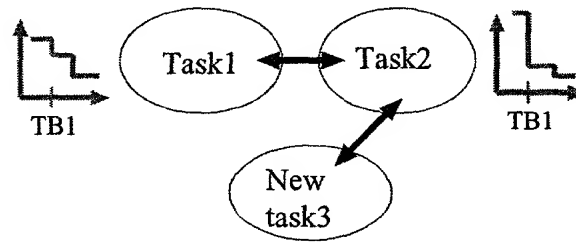


Figure 7.11: Selection of appropriate point on Pareto curves for TCM characterized task clusters, after entering a foreign task cluster from the network.

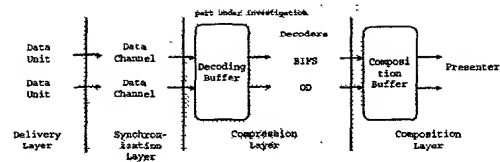


Figure 7.12: System level modules of the MPEG4 IM1 player

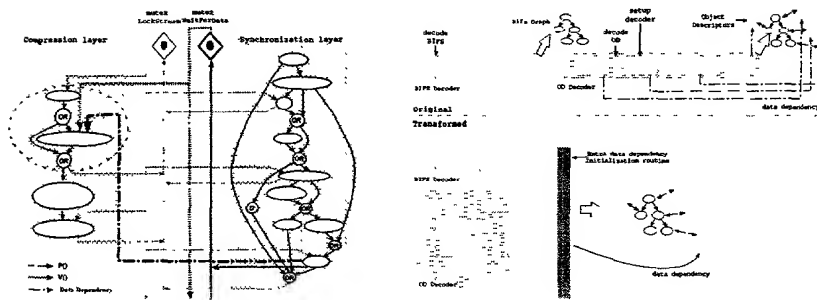


Figure 7.13: Increasing the amount of concurrency by breaking data dependencies

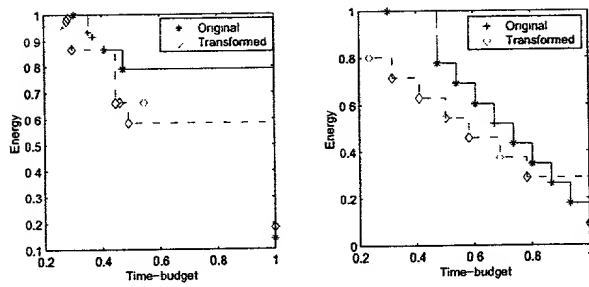


Figure 7.14: Comparison between scheduling the original and the transformed graphs

### Hierarchical rewriting hides less important constructs for TCM

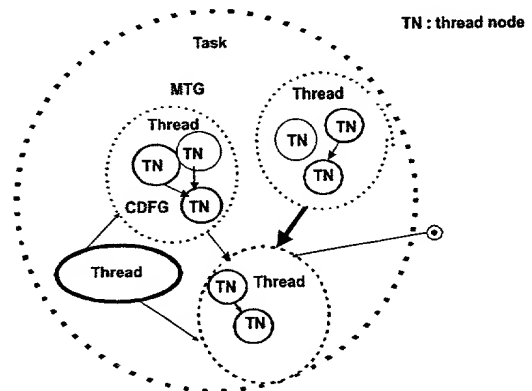


Figure 7.15: Hierarchical rewriting hides less important constructs for TCM



## Example in IM1

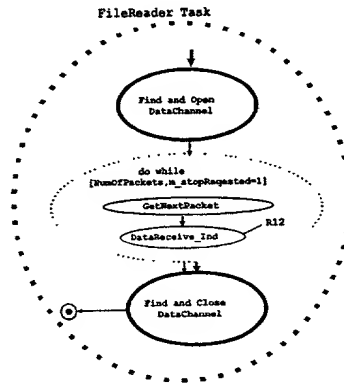


Figure 7.16: Hierarchical rewriting illustrated on IM1 player

## Hide undesired constructs without trade-off to simplify the graph

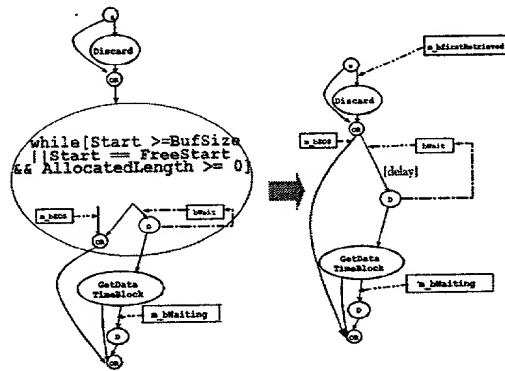


Figure 7.17: Hide undesired constructs without trade-off

## Code expansion creates freedom for scheduling

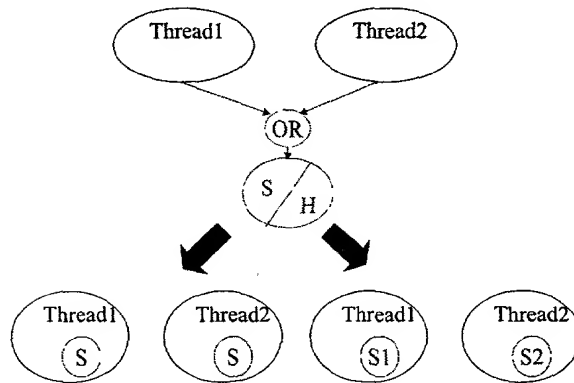


Figure 7.18: Code expansion creates freedom for scheduling

## Code expansion in IM1(1)

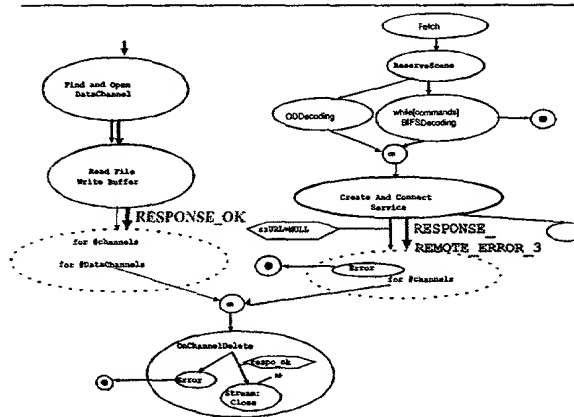


Figure 7.19: Code expansion in IM1 (1)

# Code expansion in IM1(2)

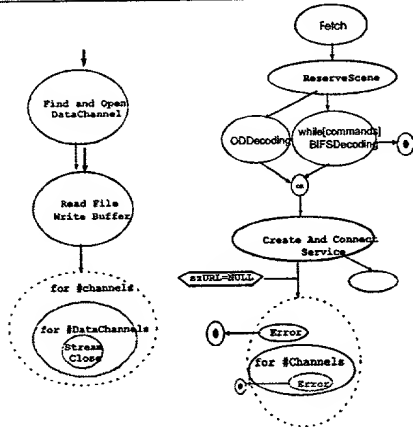


Figure 7.20: Code expansion in IM1 (2)

## Remove constructs that make concurrency analysis difficult

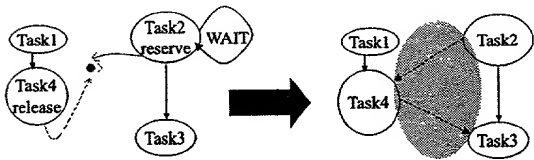


Figure 7.21: Remove constructs that make concurrency analysis difficult

## Trade-off complexity/freedom must be taken into account (1)

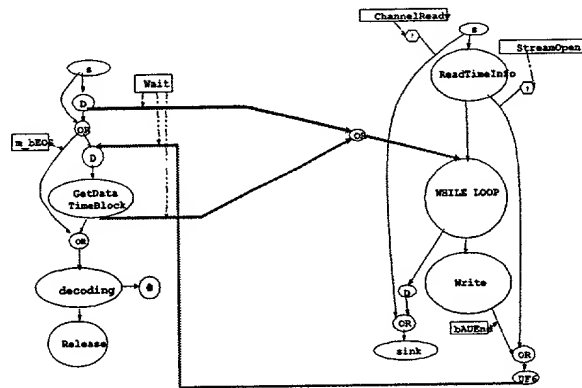


Figure 7.22: Trade-off complexity/freedom must be taken into account (1)

## Trade-off complexity/freedom must be taken into account (2)

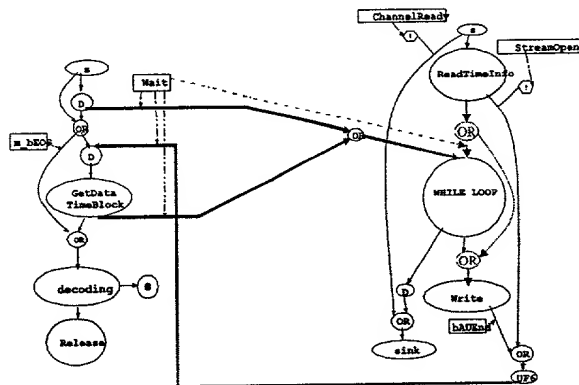


Figure 7.23: Trade-off complexity/freedom must be taken into account (2)

## Transform constructs that cannot be removed

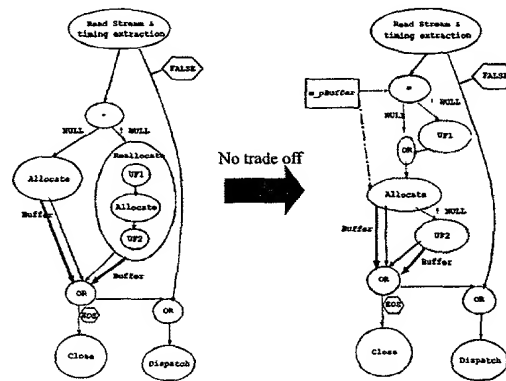


Figure 7.24: Transform constructs that cannot be removed

Concurrency analysis focuses on the parallelism

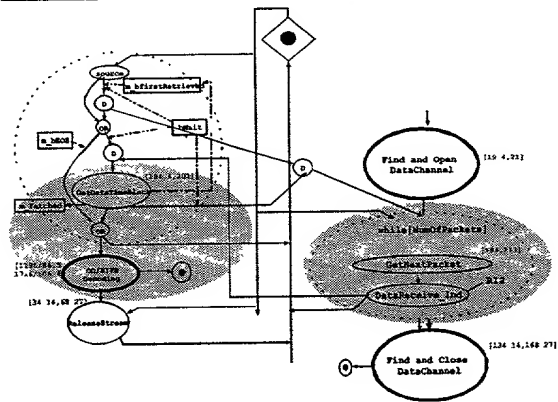


Figure 7.25: Concurrency analysis focuses on parallelism

# Remove unused or redundant code

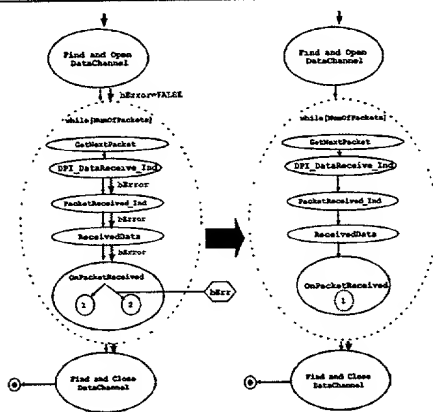


Figure 7.26: Remove unused or redundant code

# Weight-based hiding reduces complexity further with trade-off

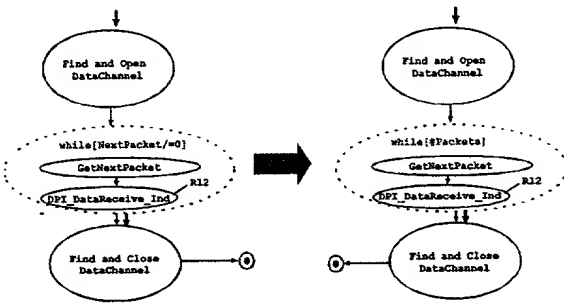


Figure 7.27: Weight-based hiding reduces complexity further with trade-off

Partitioning clusters tasks with high interaction

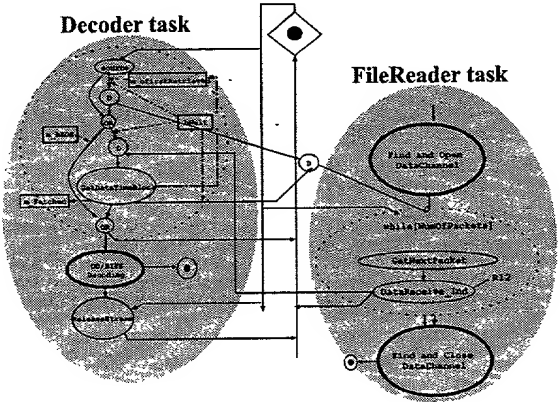


Figure 7.28: Partitioning clusters tasks with high interaction

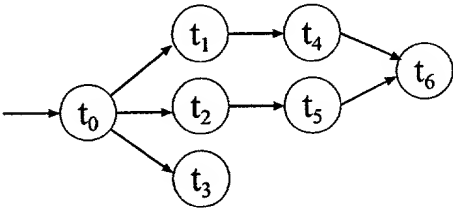


Figure 7.29: An example of a task graph.

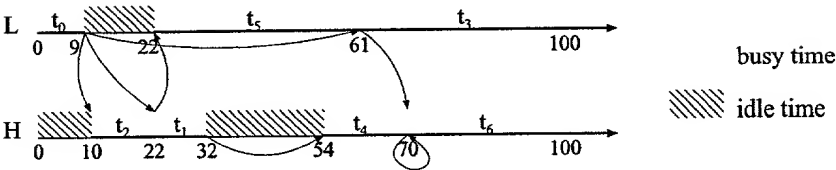


Figure 7.30: Static scheduling result.



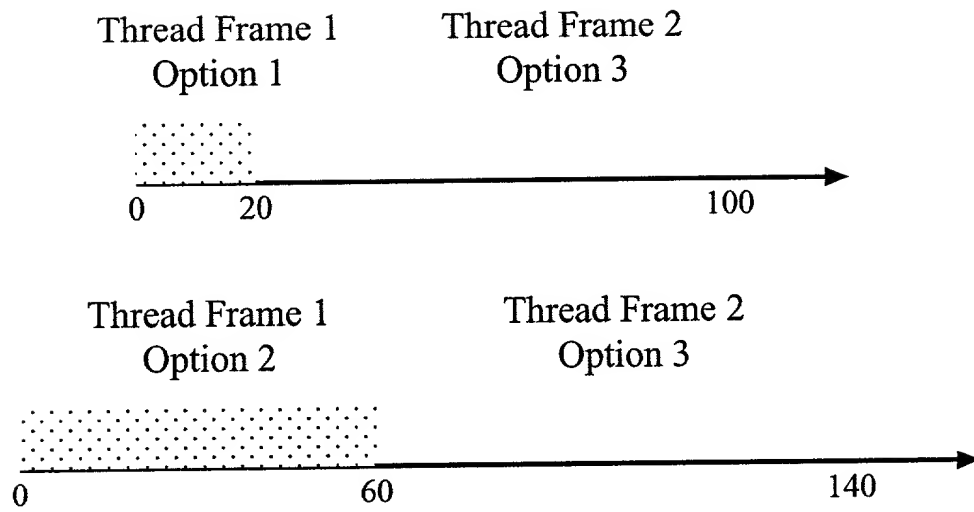


Figure 7.31: Dynamic scheduling of two example thread frame.

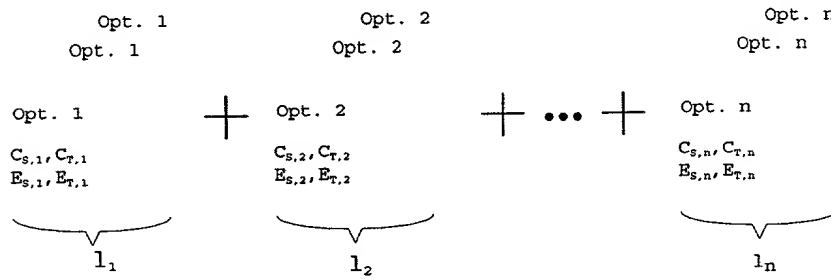


Figure 7.32: The dynamic scheduling of ADSL.

FORBIDDEN

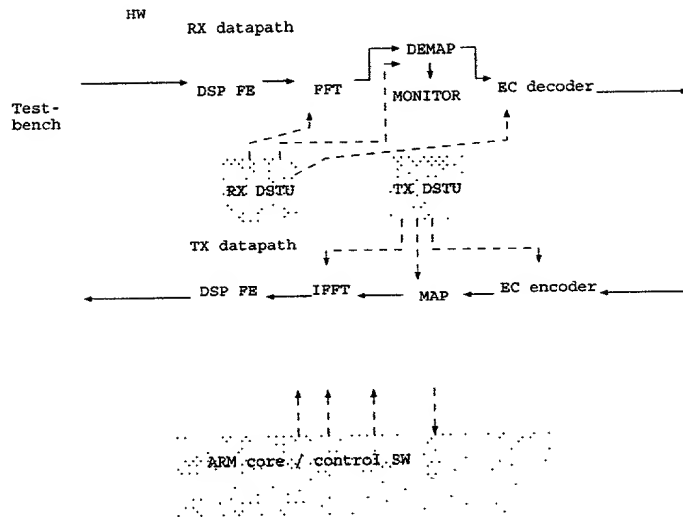


Figure 7.33: ADSL digital modem schematic.

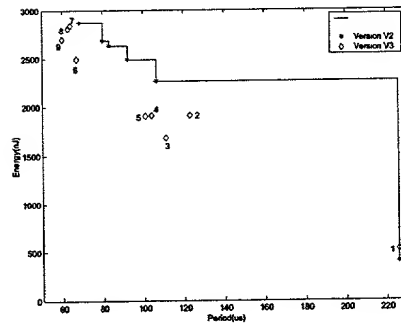


Figure 7.34: Comparison between scheduling the initial and the second transformed graphs

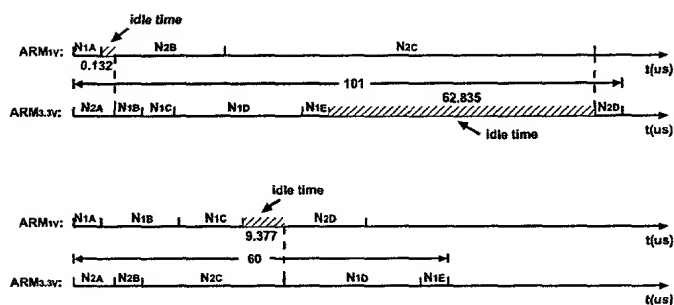


Figure 7.35: Examples of scheduling the second transformed graph

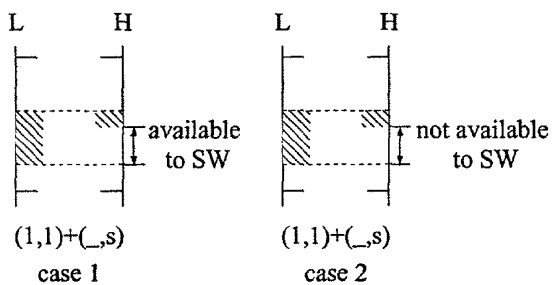


Figure 7.36: The difference between case 1 and case 2.

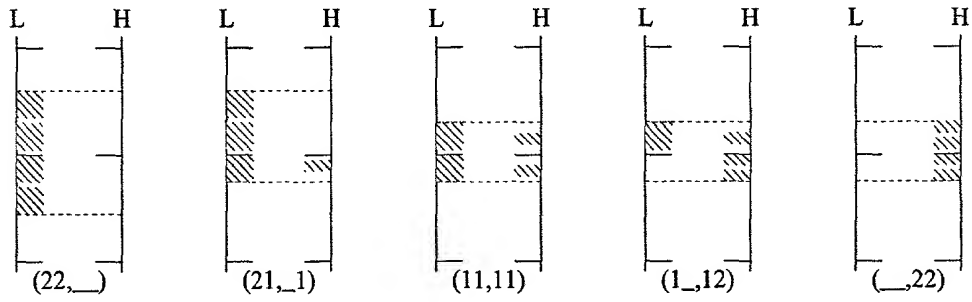


Figure 7.37: All possible schedules of the timers in case 3.

	Execution Time							Energy Consumption						
	$t_0$	$t_1$	$t_2$	$t_3$	$t_4$	$t_5$	$t_6$	$t_0$	$t_1$	$t_2$	$t_3$	$t_4$	$t_5$	$t_6$
P1(H)	3	10	12	13	16	13	30	27	90	108	117	144	117	270
P2(L)	9	30	36	39	48	39	90	3	10	12	13	16	13	30

Table 7.1: Thread nodes performance.

	Thread Frame One			Thread Frame Two		
	opt.1	opt.2	opt.3	opt.1	opt.2	opt.3
Cycle Budget	20	60	100	40	60	80
Energy Cost	110	80	50	90	60	50

Table 7.2: Two example thread frames.

Vdd	1 V	3 V	4 V	5 V
Frequency	10MHz	30MHz	40MHz	50MHz
Power (normalized)	1	27	64	125

Table 7.3: Assumption on processors.

Task	4	5	6	7	8	9	10	11	12	14	15	16	17	18
Deadline (symbol)	128	96	128	128	768	256	128	132	16	64	16	2048	64	576
Ex. Time (ms)(10MHz)	3	3	3	21	240	9	60	12	3	21	3	864	18	285

Table 7.4: Dead line and execution time of SW tasks.

(L,H)	1,1		2,-		-,2	
	s,-	-,s	s,-	-,s	s,-	-,s
Eq. $C_{S,i}(\mu s)$	166	624	102	690	230	564
$E_{S,i} + E_{T,i}(\times 10^{-6})$	797	6247	230	6338	1364	6210

Table 7.5: Execution time and energy consumption in one TB , case 1.

(L,H)	1,1		2,-		-,2		Energy ( $\times 10^{-6}$ )
	s,-	-,s	s,-	-,s	s,-	-,s	
task4			30				6900
task7	1		65		62		100315
task8	1			138	629		$1.73 \times 10^6$
task9			89				20470
task10			2	67	59		505582
task11			3	11	18		94960
task12			5		11		16154
task14			1	14	49		155798
task16	1		2	855	1190		$7.04 \times 10^6$
task17			3	8	53		123686
task18	1		1	332	242		$2.44 \times 10^6$
Total							$1.22 \times 10^7$

Table 7.6: Scheduling result, case 1.

(L,H)	1,1		2,-		-,2	
	s,-	-,s	s,-	-,s	s,-	-,s
Eq. $C_{S,i}(\mu s)$	166	498	102	306	188	564
$E_{S,i} + E_{T,i}(\times 10^{-6})$	797	5113	230	2882	1322	6210

Table 7.7: Execution time and energy consumption in one TB , case 2.

(L,H)	1,1		2,-		-,2		Energy ( $\times 10^{-6}$ )
	s,-	-,s	s,-	-,s	s,-	-,s	
task4			30				6900
task7	123		4		1		100273
task8	429	339					$2.075 \times 10^6$
task9			89				20470
task10	10	117	1				606421
task11	12	19				1	112921
task12	14	1			1		17593
task14	32	30			1	1	186426
task16	467	1579		2			$8.45 \times 10^6$
task17	40	22	1	1			147478
task18	4	570		1	1		$2.92 \times 10^6$
Total							$1.464 \times 10^7$

Table 7.8: Scheduling result, case 2.

(L,H)	22,-		21,-1		11,11		1-,12		-,22	
	s,-	-,s	s,-	-,s	s,-	-,s	s,-	-,s	s,-	-,s
Eq. $C_{S,i}(\mu s)$	204	612	268	804	332	996	352	1056	376	1128
$E_{S,i} + E_{T,i}(\times 10^{-6})$	460	5764	1027	7975	1594	10226	2117	11269	2644	12420

Table 7.9: Execution time and energy consumption in one TB , case 3.



(L,H)	222,--		221,--1		121,1_1		12,1_2		2,2_2		Energy ( $\times 10^{-6}$ )
	s,-	-s	s,-	-s	s,-	-s	s,-	-s	s,-	-s	
task4	15										8820
task7					33	7	1		1		260100
task8		1			99	154	1	1			$3.93 \times 10^6$
task9	45										26460
task10						25		1		16	$1.09 \times 10^6$
task11				1	1	8					209548
task12	1	1			2	1					42852
task14					5	14	1		1		351156
task16					41	639	1	1			$1.52 \times 10^7$
task17					8	11	1		1		288408
task18						74		1		117	$5.23 \times 10^6$
Total											$2.665 \times 10^7$

Table 7.12: Scheduling result, case 4.

(L,H)	222,--		221,--1		121,1_1		12,1_2		2,2_2	
	s,-	-s	s,-	-s	s,-	-s	s,-	-s	s,-	-s
Eq. $C_{S,i}(\mu s)$	204	1020	268	1340	332	1660	370	1850	408	2040
$E_{S,i} + E_{T,i}(\times 10^{-6})$	716	26012	2065	35297	3710	44878	5309	51189	6908	57500

Table 7.13: Execution time and energy consumption in one TB , case 5.

(L,H)	222,--		221,--1		121,1_1		12,1_2		2,2_2		Energy ( $\times 10^{-6}$ )
	s,-	-s	s,-	-s	s,-	-s	s,-	-s	s,-	-s	
task4	15										10740
task7				1	23	7			1		441681
task8			1	1	57	132	1				$6.18 \times 10^6$
task9	45										32220
task10				1				24		7	$1.67 \times 10^6$
task11				4		4					320700
task12			1		1		1			1	68584
task14				1	3	11			1		546993
task16				1		437		72		2	$2.34 \times 10^7$
task17				6	5	5					454722
task18								46		98	$7.99 \times 10^6$
Total											$4.11 \times 10^7$

Table 7.14: Scheduling result, case 5.

Case Number	1	2	3	4	5
Total Energy Cost	12.2	14.64	14.64	26.65	41.1

Table 7.15: Energy cost of different cases at different working voltages.



Case Number	1	2	3	4	5
Total Energy Cost	31.2	34.6	34.6	39.1	41.1

Table 7.16: Energy cost of different cases at the same working voltages.

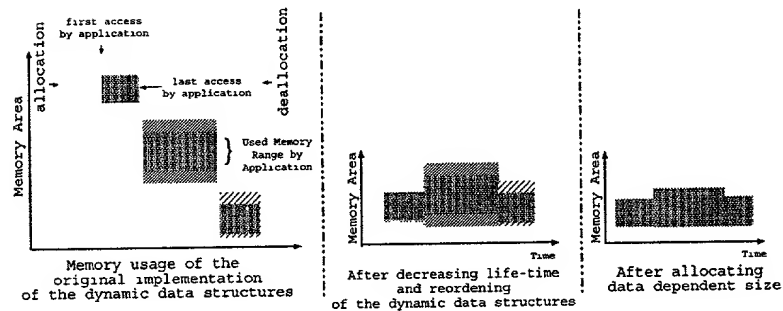


Figure 7.38: DM oriented transformations illustrated on the input buffers of the IM1-player

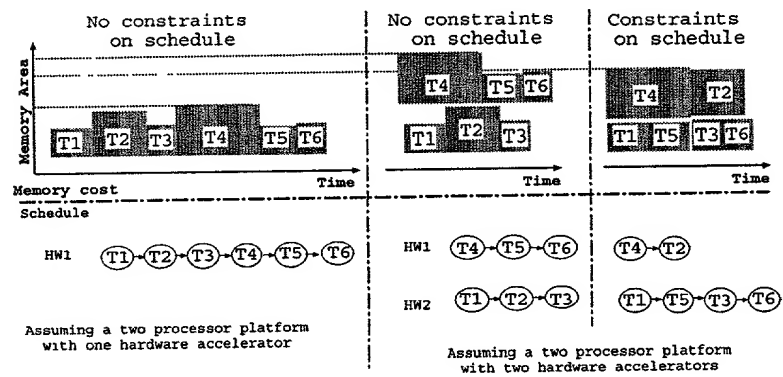


Figure 7.39: Constraints on the task-schedule reducing the DM requirements of a system

Table 7.17: Execution times and processing energy of most important tasks in IM1-player on a heterogeneous platform with one and two hardware accelerators

	1 HW accelerator		2 HW accelerators	
	Execution Time	Processor Energy	Execution Time	Processor Energy
OD	9ms	0.37mJ	9ms	0.37ms
BIFS	24ms	0.98mJ	24ms	0.98mJ
Delivery	8.1ms	0.32mJ	16.2ms	0.64mJ
Wavelet	30ms	1mJ	30ms	2mJ
Total	30ms	2.58mJ	30ms	4mJ

Table 7.18: Memory requirements and memory energy of most important tasks in IM1-player on a heterogeneous platform with one and two hardware accelerators

	1 HW accelerator			2 HW accelerators		
	Mem. Accesses	Mem. Size Pre	Mem. Size Post	Mem. Accesses	Mem. Size Pre	Mem. Size Post
OD	0.58k	10kB	0.58kB	0.58kB	10kB	0.58kB
BIFS	2.41k	41kB	2.41kB	2.41k	41kB	2.41kB
Delivery	35.9k	35.9Bk	12.4kB	71.8k	71.8kB	17kB
Wavelet	35.9k	35.9kB	12.4kB	71.8k	71.8kB	17kB
Total	74.9k	86.9kB	14.8k	146k	193kB	19.4k

1 HW accelerator		2 HW accelerators	
Energy Pre	Energy Post	Energy Pre	Energy Post
0.78mJ	0.16mJ	1.54mJ	0.19mJ